CLAIMS

WHAT IS CLAIMED:

1. A method of forming a semiconductor device feature, the method comprising:

providing a substrate having a first layer formed thereon;

covering said substrate with a second layer of material;

implanting ions into said second layer of material to modify a structure of the material of said second layer;

patterning said second layer of material and said first layer by photolithography to form said semiconductor device feature in said first layer; and

removing said patterned second layer of material, whereby a selectivity in removing said patterned second layer is increased by the implanting of said ions.

2. The method of claim 1, wherein said ions are substantially inert ions.

3. The method of claim 1, wherein said ions are at least one of argon ions, xenon ions, germanium ions and silicon ions.

4. The method of claim 1, wherein the ion dose is in the range of approximately 1×10^{13} to 5×10^{15} ions/cm^2.

5. The method of claim 1, wherein the ion energy is in the range of approximately 5-80 keV.

6. The method of claim 1, wherein said layer of material is an anti-reflective coating layer.

7. The method of claim 1, wherein said layer of material is comprised of an inorganic material.

8. The method of claim 1, wherein the material of said layer of material is one of silicon nitride and silicon reacted nitride.

9. The method of claim 1, wherein a dimension of the device feature in one direction is 100 nm or less.

10. A method of forming a semiconductor device structure, the method comprising:

providing a substrate having formed thereon at least one partially formed semiconductor device, wherein said partially formed semiconductor device comprises at least one feature with sidewalls and sidewall spacers formed thereon;

implanting ions into said sidewall spacers by performing an angled ion implantation process; and

removing a patterned layer of material, whereby a selectivity in removing said patterned layer is increased by the implanting of said ions.

11. The method of claim 10, wherein providing a substrate further comprises forming said sidewall spacers at the sidewalls of at least one feature of said partially formed

semiconductor device by covering said substrate with a layer of material and by patterning the layer of material in an anisotropic etch process.

12. The method of claim 11, wherein providing a substrate further comprises forming said sidewall spacers at said sidewalls of said at least one feature of said partially formed semiconductor device, and wherein the method further comprises implanting dopants into said substrate to form a region of enhanced conductivity in the semiconductor device after the formation of sidewall spacers.

13. The method of claim 12, wherein said region of enhanced conductivity comprises at least source/drain regions.

14. The method of claim 10, wherein a tilt angle between a surface of said substrate and the direction of incidence of said ions is in the range of approximately 10-85 degrees.

15. The method of claim 10, wherein said ions are substantially inert ions.

16. The method of claim 10, wherein said ions are at least one of argon ions, xenon ions, germanium ions and silicon ions.

17. The method of claim 10, wherein the ion dose is in the range of approximately 1×10^{13} to 5×10^{15} ions/cm^2.

18. The method of claim 10, wherein the ion energy is in the range of approximately 10-80 keV.

19. The method of claim 10, wherein the material of said sidewall spacers comprises an inorganic material.

20. The method of claim 10, wherein the material of said sidewall spacers comprises silicon nitride.

21. The method of claim 10, wherein a dimension of said at least one feature in one direction is 100 nm or less.